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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : K. Shepard
Serial No. : 09/591,270 Examiner: To Be Assigned
Filed : June 9, 2000 Group Art Unit: 2858
For : METHODS FOR ESTIMATING THE BODY VOLTAGE OF DIGITAL
PARTIALLY DEPLETED SILICON-ON-INSULATOR CIRCUITS

INFORMATION DISCLOSURE STATEMENT

I hereby certify that this paper is being deposited with the
United States Postal Service as First Class Mail in an
envelope addressed to: Assistant Commissioner for
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August 17, 2001

Date of Deposit

Paul A. Ragusa

Attorney Name

Signature

38,587

Registration No.

August 17, 2001

Date of Signature

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §1.56, 37 C.F.R. §1.97 and 37 C.F.R. §1.98, Applicants, by
their attorneys, hereby bring the following documents, to the attention of the Examiner in
connection with the examination of the above-captioned patent application:


PATENT

1. Lu et al., "Floating-body Effects in Partially SOI CMOS circuits", 32 IEEE J. Solid-Stated Circuits 1241 (1997).
2. D.H. Allen et al., "A 0.20 μ m 1.8 V SOI 550 MhZ 64b Power PC Microprocessor with Cu Interconnects", Digest Tech. Papers, ISSCC, pp. 438-39, (1999).
3. C.T. Chuang et al., "SOI Digital CMOS VLSI – A Design Perspective", 36th ACM/IEEE Design Automation Concerence, pp.709-714, (1999).
4. J. Gautier et al., "On the Transient Operation of Partially Depleted SOI NMOSFET's", 16 IEEE Electron Device Letters 498 (1995).
5. R. Puri et al., "Hysteresis Effect in Pass-Transistor-Based Partially-Depleted SOI CMOS Circuits", Proc. Int'l SOI Conf., 1998.

A copy of the Chuang et al. article is not readily available. A copy will be forwarded to the Patent Office upon our receipt of same. A PTO-1449 form and a copy of each of the remaining above-listed documents are enclosed.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 02-4377.

Respectfully submitted,



Paul A. Ragusa
Patent Office Reg. No. 38,587
Attorneys for Applicants
(212) 408-2588

Enclosures